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1 Fast hardware-software coverification by optimistic execution of real processor

Sungjoo Yoo, Jong-Eun Lee, Jinyong Jung, Kyungseok Rha, Youngchul Cho, Kiyoung Choi

January 2000 DATE '00: Proceedings of the conference on Design, automation and test in Europe

Publisher: ACM

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Additional Information: full citation, references, index terms

2 A fast hardware/software co-verification method for system-on-a-chip by using a C/C++ simulator and FPGA emulator with shared register communication

Yuichi Nakamura, Kouhei Hosokawa, Ichiro Kuroda, Ko Yoshikawa, Takeshi Yoshimura

June 2004 DAC '04: Proceedings of the 41st annual conference on Design automation

Publisher: ACM

Full text available: pdf(1.03 MB)

Additional Information: full citation, abstract, references, cited by, index terms, review

This paper describes a new hardware/software co-verification method for System-On-a-Chip, based on the integration of a C/C++ simulator and an inexpensive FPGA emulator. Communication between the simulator and emulator occurs via a flexible interface ...

Keywords: C/C++ simulator, FPGA emulation, co-verification

3 How to make efficient communication, collaboration, and optimization from system to chip

Akira Matsuzawa

June 2003 DAC '03: Proceedings of the 40th conference on Design automation

Publisher: ACM

Full text available: pdf(142.40 KB)

Additional Information: full citation, references, index terms

Keywords: CMOS, LSI, SoC, circuit design, mixed signal

4 ESL design and HW/SW co-verification of high-end software defined radio platforms

A. C. H. Ng, J. W. Weijers, M. Glassee, T. Schuster, B. Bougard, L. Van der Perre

September 2007 CODES+ISSS '07: Proceedings of the 5th IEEE/ACM international conference on Hardware/software codesign and system synthesis

Publisher: ACM

Full text available: pdf(345.90 KB) Additional Information: full citation, abstract, references, index terms

Multiple wireless technologies are converging to run on personal handhelds. The plethora of communication standards next to the cost issues of deeper submicron processing require handheld platforms to shift from sets of multiple application specific ...

Keywords: ESL, SDR, emulation, hardware/software co-design, verification

5 A chip prototyping substrate: the flexible architecture for simulation and testing (FAST)

John D. Davis, Stephen E. Richardson, Charis Charitsis, Kunle Olukotun

November 2005 ACM SIGARCH Computer Architecture News, Volume 33 Issue 4

Publisher: ACM

Full text available: pdf(333.79 KB) Additional Information: full citation, abstract, references, cited by, index terms

We describe a hybrid hardware emulation environment: the Flexible Architecture for Simulation and Testing (FAST). FAST integrates field-programmable gate arrays (FPGAs), microprocessors, and memory to enable rapid prototyping of chip multiprocessors, ...

6 Proceedings of the conference on Design, automation and test in Europe

Rudy Lauwereins, Jan Madsen

April 2007 proceeding

Publisher: EDA Consortium

Additional Information: full citation, abstract

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7 Accelerating system-on-chip power analysis using hybrid power estimation

Mohammad Ali Ghodrat, Kanishka Lahiri, Anand Raghunathan

June 2007 DAC '07: Proceedings of the 44th annual conference on Design automation

Publisher: ACM

Full text available: pdf(630.91 KB) Additional Information: full citation, abstract, references, index terms

Fast and accurate power analysis is a critical requirement for designing power-efficient System-on-Chips (SoCs). Current system-level power analysis tools are incapable of generating power estimates under real-life workloads within an acceptable amount ...

Keywords: emulation, power analysis, power estimation, simulation, system-on-chip

8 Cycle Accurate Binary Translation for Simulation Acceleration in Rapid Prototyping of SoCs

Jurgen Schnerr, Oliver Bringmann, Wolfgang Rosenstiel
March 2005 DATE '05: Proceedings of the conference on Design, Automation and Test in Europe - Volume 2, Volume 2
Publisher: IEEE Computer Society
Full text available: pdf(138.92 KB) Additional Information: full citation, abstract, index terms

In this paper, the application of a cycle accurate binary translator for rapid prototyping of SoCs will be presented. This translator generates code to run on a rapid prototyping system consisting of a VLIW processor and FPGAs. The generated code is ...

9 An Assembler Driven Verification Methodology (ADVM)

John S. MacBeth, Dietmar Heinz, Ken Gray
March 2005 DATE '05: Proceedings of the conference on Design, Automation and Test in Europe - Volume 3, Volume 3
Publisher: IEEE Computer Society
Full text available: pdf(664.85 KB) Additional Information: full citation, abstract, index terms

This paper presents an overview of an assembler driven verification methodology (ADVM) that was created and implemented for a chip card project at Infineon Technologies AG. The primary advantage of this methodology is that it enables rapid porting of ...

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